We claim:

1. A method comprising:

detecting a correctable error while processing a transaction within a pipeline;

outputting the transaction from the pipeline into an error queue;

processing a correction command within the pipeline to correct the correctable error within the transaction; and,

reprocessing the transaction within the pipeline, where the correctable error therewithin has been corrected.

2. The method of claim 1, further comprising, prior to processing the correction command, inputting the correction command into the pipeline.

3. The method of claim 2, further comprising, prior to inputting the correction command into the pipeline, operating the pipeline in a correction mode.

4. The method of claim 1, further comprising, prior to reprocessing the transaction within the pipeline, inputting the transaction from the error queue back into the pipeline.

5. The method of claim 4, further comprising, prior to inputting the transaction from the error queue back into the pipeline, operating the pipeline in a restart mode.

6. The method of claim 1, further comprising, after reprocessing the transaction within the pipeline, operating the pipeline in a normal mode.

7. A system comprising:

a plurality of nodes interconnected to one another, each node comprising:

a plurality of processors;

local random-access memory (RAM) for the plurality of processors; and,

at least one controller to process transactions relating to the local RAM of the node, including correcting correctable errors within the transactions in a non-inline manner in a separate correction mode.

8. The system of claim 7, wherein each controller comprises a pipeline in which the transactions are processed and that includes logic to detect the correctable errors within the transactions.

9. The system of claim 7, wherein each controller comprises a mode controller to control a current mode in which the controller is operating.

10. The system of claim 7, wherein each controller comprises an error queue to which those of the transactions including the correctable errors are routed for correction and reprocessing.

11. The system of claim 7, wherein each controller includes a normal mode in which the transactions are processed and a restart mode in which those of the transaction including the correctable errors are reprocessed after correction of the correctable errors.

12. The system of claim 7, wherein each controller of each node comprises an application-specific integrated circuit (ASIC).

13. A controller for a node of a system comprising:

a pipeline in which transactions are processed;

a mode controller to control a mode in which the pipeline operates; and,

an error queue to which those of the transactions including correctable errors are routed for correction of the correctable errors and reprocessing of the transactions.

14. The controller of claim 16, wherein the mode in which the pipeline operates includes one of a normal mode, a correction mode, or a restart mode.

15. The controller of claim 13, wherein the mode controller switches the operation of the pipeline in the normal mode for processing those of the transactions not including the correctable errors.

16. The controller of claim 13, wherein the mode controller switches the operation of the pipeline in the correction mode for correcting the correctable errors within those of the transactions including the correctable errors.

17. The controller of claim 13, wherein the mode controller switches the operation of the pipeline in the restart mode for processing those of the transactions including the correctable errors after the correctable errors have been corrected.

18. A controller for a node of a system comprising:

a pipeline in which transactions are processed;

a mode controller to control a mode in which the pipeline is operable as one of a normal mode, a correction mode, and a restart mode; and,

an error queue to which those of the transactions including correctable errors are routed for correction of the correctable errors and reprocessing of the transactions.

19. A system comprising:

a plurality of nodes interconnected to one another, each node comprising:

a plurality of processors;

local random-access memory (RAM) for the plurality of processors; and,

at least one controller to process transactions relating to the local RAM of the node, including correcting correctable errors within the transactions in a non-inline manner in a separate correction mode, each controller having a pipeline in which the transactions are processed and that includes logic to detect the correctable errors within the transactions.